# Maharashtra State Board of Technical Education, Mumbai

**K-1**

# TEACHING PLAN (TP)/CIS

**Academic Year: 2026-2027**

**Date: 01/07/2026**

**Institute Name &Code:** K. K. Wagh Polytechnic, Nashik (0078)
**Program Name and Code:** Information Technology (IF) **Course Index:** 304
**Course Name:** Digital Techniques and Microprocessors (DTM)
**Course Abbreviation and Code:** DTM-313305 **Semester**: III[rd] **Scheme**: 'K'
**Allocated Hrs: 45** **Name of Faculty:** Mr. R.J.Shinde
**Class:** CRAY

## • Teaching-Learning and Assessment Scheme:

| Course Code | Course Title | Abbr | Course Category/s | Learning Scheme | | | | | Credits | Assessment Scheme | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Actual Contact Hrs./Week | | | SLH | NLH | | Paper Duration | Theory | | | | Based on LL & TL | | | | Based on SL | | Total Marks |
| | | | | | | | | | | | | | | | Practical | | | | | | |
| | | | | CL | TL | LL | | | | | FA-TH | SA-TH | Total | | FA-PR | | SA-PR | | SLA | | |
| | | | | | | | | | | | Max | Max | Max | Min | Max | Min | Max | Min | Max | Min | |
| 313305 | DIGITAL TECHNIQUES AND MICROPROCESSORS | DTM | AEC | 3 | - | 2 | 1 | 6 | 3 | 3 | 30 | 70 | 100 | 40 | 25 | 10 | 25@ | 10 | 25 | 10 | 175 |

## • Course Outcomes (COs) & Theory Learning Outcomes (TLOs):

By learning the course Digital Techniques and Microprocessor (DTM -313305) Second year IF students will be able to:

| CO No. | TLO's No. | Course Outcomes (COs) / Theory Learning Outcomes (TLO's) |
|---|---|---|
| **CO304.1** | | **Number Systems and Digital Logic Gates** |
| | TLO 1.1 | TLO 1.1 Convert the givennumber system to the specified number system. |
| | TLO 1.2 | Convert given formof code to another code. |
| | TLO 1.3 | Apply arithmeticoperations on the numberbelong to given number system. |
| | TLO 1.4 | Derive the truth tableof the given basic logic gates /derived logic gates |
| | TLO 1.5 | Design the logicalcircuit for the given application. |
| **CO304.2** | | **Combinational and Sequential LogicCircuits** |
| | TLO 2.1 | Explain concept ofSum-of- Product (SOP) andProduct-of-Sum(POS). |
| | TLO 2.2 | Explain concept ofhalf-full adder / half-full subtractor using K-MAP. |
| | TLO 2.3 | Construct the logicaldiagrams using multiplexer / demultiplexer ICs to solve the given expression. |
| | TLO 2.4 | State the use of latch,flipflop, counter, buffer. |
| **CO304.3** | | **16-Bit Microprocessor 8086** |
| | TLO 3.1 | Enlist features of8086 microprocessor. |
| | TLO 3.2 | Calculate physicaladdress to locate the given data from memory segmentation. |
| | TLO 3.3 | Explain given blocksof architecture of 8086 microprocessor |
| | TLO 3.4 | Compare minimummode and maximum mode of 8086 features. |
| **CO304.4** | | **Basic assembly Language Programmingusing 8086** |
| | TLO 4.1 | TLO 4.1 Identify relevantaddressing mode of instruction. |
| | TLO 4.2 | Choose relevantinstruction to perform thegiven operation from theinstruction set of |

| | | |
|---|---|---|
| | | 8086. |
| | TLO 4.3 | Use data transfer andarithmetic instruction for given situation employing specific addressing mode. |
| | TLO 4.4 | Use logical and flagmanipulation instruction for given situation employing specific addressing mode |
| **CO304.5** | | **Assembly Language Programming usingLoops and Branching instructions** |
| | TLO 5.1 | Develop the assembly language program to solve the given problem usinglooping. |
| | TLO 5.2 | Develop the assembly language program to solve the given problem usingbranching structure. |

- **Teaching Plan:**

| Unit No. (Allotted Hrs. & Marks ) | COs & TLOs | Unit Title with Topic Details/Contents | Plan Dates (From-To & No. of Lectures) | Actual Execution (From-To & No. of Lectures) | Teaching Method/ Media | Remark |
|---|---|---|---|---|---|---|
| 01 (08) 12 Marks | CO1 TLO 1.1 | **Unit – I Number Systems and Digital Logic Gates** Terms - Bit, Byte, Nibble, Word | 01/07/2026 (01) | | Chalk-Board, LCD+PPTs, eNotes, Ref. Book | |
| | 1.2 | Number systems- Decimal, Binary, Octal, Hexadecimal and their conversions from one numbersystem to another | 03/07/2026 06/07/2026 (02) | | Chalk-Board, LCD+PPTs | |
| | 1.3 | Codes and code conversion: BCD, GRAY, ASCII,EBCDIC | 08/07/2026 (01) | | Chalk-Board, LCD+PPTs, | |
| | 1.4 | Binary, Hexadecimal, BCD arithmetic and 1's and 2's complement (up to 8 bit) | 10/07/2026 (01) | | Chalk-Board, Ref. Book | |
| | 1.5 | Basic logic gates(AND,OR,NOT), universal gates (NAND,NOR), special gates (EX-OR, EX-NOR), and their truth table, basic gates using universal gates | 13/07/2026 15/07/2026 (02) | | Chalk-Board, LCD+PPTs, eNotes, YouTube Videos | |
| | 1.6 | Basic logic operations using laws of Boolean algebra, De-Morgan's theorems | 17/07/2026 (01) | | Chalk-Board, LCD+PPTs, | |
| 02 (10) 16 Marks | CO2 TLO-2.1 | **Unit – II Combinational and Sequential Logic Circuits** Standard/canonical forms for Boolean functions, Min-terms and Max-terms, Minimization of expressionusing SOP-POS and K-MAP, simplification of expression of half adder/full adder and half/full subtractor using K-MAPs | 20/07/2026 22/07/2026 24/07/2026 (03) | | Chalk-Board, LCD+PPTs, eNotes, YouTube Videos | |
| | 2.2 | Concept of multiplexer and demultiplexer, logicaldiagram development using multiplexer/ demultiplexerICs | 27/07/2026 29/07/2026 (02) | | Chalk-Board, LCD+PPTs, YouTube Videos | |
| | 2.3 | Multiplexer tree and demultiplexer tree,applications of multiplexers and demultiplexers | 31/07/2026 03/08/2026 (02) | | Chalk-Board, eNotes, | |

| | | | | | | |
|---|---|---|---|---|---|---|
| | 2.4 | Clock signal, flipflop, latches, counter, buffer andtri-state buffer (only concept | 05/08/2026<br>07/08/2026<br>14/08/2026<br>(03) | | Chalk-Board, LCD+PPTs, eNotes, MKCL ERA, YouTube Videos | |
| 03<br>(08)<br>12<br>Marks | CO3<br>TLO-3.1 | **Unit - III 16-Bit Microprocessor 8086**<br>Microprocessor 8086 features, pin diagram description and architecture of 8086 | 17/08/2026<br>19/08/2026<br>(02) | | Chalk-Board, LCD+PPTs, eNotes, YouTube Videos | |
| | 3.2 | Units of 8086: Bus interface unit and execution unit, concept of memory segmentation and pipelining,physical address generation | 21/08/2026<br>24/08/2026<br>(02) | | Chalk-Board, LCD+PPTs | |
| | 3.3 | Flag register of 8086, segment registers, indexregister, ALU-arithmetic logic unit | 26/08/2026<br>28/08/2026<br>(02) | | Chalk-Board, LCD+PPTs, | |
| | 3.4 | Minimum mode and maximum mode configurationof 8086, timing diagrams concept | 31/08/2026<br>02/09/2026<br>(02) | | Chalk-Board, LCD+PPTs, eNotes | |
| 04<br>(10)<br>16<br>Marks | CO4<br>TLO-4.1, | **Unit - IV Basic assembly Language Programmingusing 8086**<br>Programming model of 8086 assembly languageprogram assembler directives | 04/09/2026<br>07/09/2026<br>(02) | | Chalk, Blackboard, LCD Projector, PPT | |
| | 4.2 | Addressing modes of 8086, register, direct, based,indexed, based-indexed addressing, assembler directives | 09/09/2026<br>11/09/2026<br>16/09/2026<br>(03) | | Chalk-Board, LCD+PPTs | |
| | 4.3 | Format of instruction, instruction set: data transfer,arithmetic, logical, branch and loop, flag manipulation | 18/09/2026<br>21/09/2026<br>23/09/2026<br>(03) | | Chalk-Board, LCD+PPTs | |
| | 4.4 | Shift and rotate instructions, string instructions | 28/09/2026<br>30/09/2026<br>(02) | | Chalk-Board, LCD+PPTs, | |
| 05<br>(09)<br>14<br>Marks | CO5<br>TLO-5.1, | **Unit - V Assembly Language Programming usingLoops and Branching instructions**<br>Assembly language programs for addition,subtraction, multiplication, division on hexadecimal,BCD numbers (8/16 bit) | 05/10/2026<br>05/10/2026<br>(02) | | Classroom Learning Program development toolsand simulators | |
| | 5.2 | Assembly language programs using decisionmaking | 07/10/2026<br>07/10/2026<br>(02) | | Chalk-Board, LCD+PPTs, | |
| | 5.3 | ALP using looping andbranching structure. assembly language programs forsorting, searching and block transfer (with string and | 09/10/2026<br>09/10/2026<br>16/10/2026<br>(03) | | Chalk-Board, LCD+PPTs k-Board, LCD+PPTs, | |

| | | | | | | |
|---|---|---|---|---|---|---|
| | | without string instructions) of given numbers | | | YouTube Videos | |
| | 5.4 | Assembly language programs for uppercase tolowercase, lowercase to uppercase, conversion of hexadecimal to BCD and BCD to hexadecimal | 17/10/2026 17/10/2026 (02) | | Chalk-Board, LCD+PPTs k-Board, LCD+PPTs, MKCL ERA, YouTube Videos | |

- **COs-POs & PSOs Matrix:**

| Sr.No | Unit | Unit Title | Aligned COs | Learning Hours | R-Level | U-Level | A-Level | Total Marks |
|---|---|---|---|---|---|---|---|---|
| 1 | I | Number Systems and Digital Logic Gates | CO1 | 8 | 2 | 4 | 6 | 12 |
| 2 | II | Combinational and Sequential Logic Circuits | CO2 | 10 | 2 | 8 | 6 | 16 |
| 3 | III | 16-Bit Microprocessor 8086 | CO3 | 8 | 2 | 4 | 6 | 12 |
| 4 | IV | Basic assembly Language Programming using 8086 | CO4 | 10 | 4 | 6 | 6 | 16 |
| 5 | V | Assembly Language Programming using Loops and Branching instructions | CO5 | 9 | 2 | 6 | 6 | 14 |
| **Grand Total** | | | | **45** | **12** | **28** | **30** | **70** |

- **Direct Assessment Criteria:**

**Formative & Summative Assessment Criteria:**

- **Theory Assessment:**

**a) Formative assessment (TH-FA) :**

- Two offline class tests each of 30 marks will be conducted as per MSBTE guidelines. The average of two class test marks will be consider for final TH-FA(Average) out of 30 marks.

**b) Summative Assessment (TH- SA) :**

- The comprehensive End semester assessment will be done by MSBTE by a Theory written Examination for 70 marks. Question Paper and Assessment is performed by MSBTE.
- Final Theory Score out of 100 Marks will be derived as the total score as below:
  TH-SA [out of 70] + TH- FA [Average out of 30] = 100 Marks

- **Practical Assessment:**

1. Formative Assessment (FA) of each practical/experiment will be performed progressively for 25 marks. The assessment will be performed based on the Regularity in Practical Performance, Tool Selection Ability, Use of Appropriate tool to perform the Identified tasks, Algorithm/Solution developed, Quality of output achieved, Answer to sample questions and Submit report in total time.
2. Final Term Work (FA-PR) of 25 marks is calculated based on scores in Formative Assessment for all practical's/experiments as:
   Term Work Marks = (Sum of Total Marks Scored in FA / Total Number of Experiments) * 25
3. Self-learning Activities (SLA) includes Micro project / Assignment / other activities related to subject/course and it will be evaluated out of 25 Marks.
   A Summative (comprehensive) Assessment (SA-PR) of Practical will be performed as End Semester Examination (ESE). The SA-PR will be for 25 Marks with MSBTE guidelines at the end of semester. The schedule of MSBTE Practical ESE will be display on Notice board prior to examination.

- **References:**
  1. **Books:**

| Sr.No | Author | Title | Publisher with ISBN Number |
|---|---|---|---|
| 1 | Jain R.P. | Modern Digital Electronics | McGraw Hill Education , New Delhi, 2016, ISBN: 978-0070669116 |
| 2 | Leach Donald P., Malvino Albert Paul, Saha Gautam | Digital Principles and Applications 5/E | Tata McGraw Hill Education, New Delhi, ISBN: 978-0028018218 |
| 3 | Savaliya M. T. | 8086 Programming and advanced processor architecture | Wiley India New Delhi, 2013, ISBN: 978-8126530915 |
| 4 | Bhurchandi K. M., Roy A. K. | Advanced microprocessors and peripherals 3/E | Tata McGraw Hill Education, New Delhi, 2016, ISBN:9781259006135 |
| 5 | Triebel, Walter, Singh A., Avtar | The 8088 and 8086 Microprocessors | SCITECH Publications, Chennai 2015, ISBN:978-8183717021 |

**2.Software Learning Websites:**

| Sr.No | Link / Portal | Description |
|---|---|---|
| 1 | https://dld-iitb.vlabs.ac.in/ | Virtual Lab IIT, Bombay |
| 2 | https://www.falstad.com/circuit/ | Paul Falstad Circuit Simulator |
| 3 | https://logic.ly/ | Online Simulator for Digital Techniques |
| 4 | https://cse15-iiith.vlabs.ac.in/ | Virtual Lab IIT, Delhi |

**3.URLs of Referred Videos:**

| Sr. No. | Link / Portal | Description |
|---|---|---|
| 1 | https://youtu.be/0lwhoQ5aQe8?si=bY2vqIHmhr4R2_jp | Logic Gates Introduction |
| 2 | https://youtu.be/QIyugGzih4k?si=dcauWHRmoN7x_ImN | Binary Code Conversion System |
| 3 | https://youtu.be/LTtuYeSmJ2g?si=pF81TD8G7QuCTmHf | Latch & Flip Flop |
| 4 | https://youtu.be/fLN1YOmuAr8?si=t_Iu8fr0EvFtnhdf | Sequential Circuits |
| 5 | https://youtu.be/NjMX4hohyRI?si=DTAAtybNP2LCCnff | Shift Register |

1. **Tools :**
- Google Classroom used for Uploading Learning Material of Course, Assignments, Practice Test etc.
- MKCL LMS Era – Describe the use of the Tool in Leaning and Assessment

Mr. R.J.Shinde
**Name & Signature of the Faculty**

Prof. M.S.Karande
**(H.O.D IF-Dept.)**